

## REMARKS

Applicant acknowledges that Claim 17-21 are withdrawn from consideration as being drawn to a non-elected invention.

Claims 1-16 stand rejected under 35 USC § 112, second paragraph, as being indefinite. The Examiner points to the term “the silicon nitride” in various of these claims. The claims have been amended and as amended are believed to be in conformance with 35 USC § 112, second paragraph. However, note that while, in fact, the indicated claims have been amended to recite “the silicon nitride layer”, this is not in response to the rejection. Instead it is in order to conform Claims 2-9 and 11-14 to other amendments made to the respective base Claims 1 and 10. Specifically, Claim 1 has been broadened by omitting from the third clause of its body “pretreating the silicon nitride layer including”. Hence this clause of Claim 1 now reads “oxidizing the silicon nitride layer”. Hence Claims 2-9 were amended to conform to this broadening amendment to Claim 1.

Claim 1 has also been amended correspondingly, instead of referring to “the pretreated silicon nitride layer”, to say “after the oxidizing” because the “pretreating” is not longer recited in Claim 1. Hence these amendments to Claims 1-9 are not in response to a patentability rejection and are not narrowing.

Similar amendments are made to method Claim 10 and its dependent claims. Again, these amendments are not in response to a patentability rejection and are not intended to be narrowing.

Hence the rejection under § 112 is overcome.

It is noted that Claim 10 as originally filed in its fourth line said “forming a silicon nitride layer nitride”. This is believed to be a typographical error. Removal of the second occurrence of the word “nitride” from this portion of Claim 10 is to improve the form of the claim and is not narrowing and not in response to any patentability rejection.

Claim 1 stands rejected under 35 USC § 102(b) as anticipated by Takeuchi. Claim 1 has been amended so that the first clause of the body of Claim 1 now recites “forming a first layer of silicon dioxide overlying a gate electrode of the flash memory cell;”. Hence, in this respect, Claim 1 is somewhat similar to Claim 10 (which instead of reciting a gate electrode recites “a first polysilicon layer”). For the same reasons that Takeuchi does not anticipate Claim 10, Takeuchi no longer anticipates Claim 1, although Claim 1 does not have the same scope as Claim 10 since Claim 1 does not recite “a first polysilicon layer”. Hence Claim 1 distinguishes over Takeuchi. Claim 1 is therefore patentable over Takeuchi as are dependent Claims 2-9.

The Examiner indicated that Claims 2-9 and 11-14 would be allowable if amended to include limitations of the base claim and any intervening claims. Hence Applicant has submitted new Claims 22-27. Claim 22 recites the language of original Claim 1 combined with Claim 2, revised to improve the form of the claim. Claim 23 recites the language of original Claim 6 combined with base Claim 1, revised to improve the form of the claim. Similarly respectively, new Claims 24-27 claims recite respectively the language of original Claims 11-14 combined with the language of base Claim 10, again, revised to improve their form and hence all of new Claims 22 - 27 are allowable for the reasons indicated by the Examiner.

Claim 10, referred to above, was rejected under 35 USC § 103 along with Claims 15 and 16 dependent thereon as unpatentable over Hong in view of Eitan. (The amendment to the preamble of Claim 10 merely deletes unnecessary language.) In pertinent part, the Examiner stated:

However, Hong fails to teach that deposition of the second silicon oxide layer is accomplished after oxidizing the silicon nitride layer.

As Hong, Eitan describes a method to form ONO layers and teaches that the top oxide layer within an ONO layer may either be formed through an oxidation of the nitride layer or by deposition (col. 3/ll. 51-53). Eitan further teaches that forming the top oxide layer by a combination of the nitride oxidation and an oxide deposition is an alternative operation to either the nitride oxidation or the oxide deposition (col. 3/ll. 53). ...

However, the combination of Hong and Eitan, it is respectfully submitted, is not adequately motivated. The Examiner cited his motivation at page 7 of the Action:

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to oxidize Hong's nitride layer and subsequently deposit a second oxide layer on the oxidized nitride layer instead of forming the second oxide layer by either oxidizing the nitride layer or depositing an oxide layer, as taught by Eitan, since the method combining the nitride oxidation and the oxide deposition is an alternative operation to either the nitride oxidation or the oxide deposition.

While the Examiner's reasoning is not fully understood, it is assumed that the Examiner is saying that Eitan teaches forming an ONO structure. Eitan, col. 3, line 52, states "Top oxide 34 is then produced, either through an oxidation of the nitride or by deposition or by a combination thereof." The Examiner apparently believes that this meets the clause in Claim 10 (prior to the present amendment) of "pretreating the silicon nitride layer including oxidizing the silicon nitride;". Further it is understood that the Examiner would say that even with the present amendments to Claim 10, Eitan in combination with Hong would meet the recitation in Claim 10 of "oxidizing the silicon nitride layer;".

However, it is respectfully submitted that the combination of these two references by the Examiner does not have adequate motivation and hence the §103 rejection should be withdrawn.

The most relevant precedent appears to be *In re Sang Su Lee*, 277 F3d 1338 (Fed. Cir. 2000). This case states the standard to be followed in combining references for a § 103 rejection and the degree of motivation required. The case states at 1343 "When patentability

turns on the question of obviousness, the search for an analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. Further, at 1343-1344 the case states "This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. "

In the present situation, it is not seen where the motivation is found by the Examiner either in Eitan or Hong (or elsewhere in the prior art) to specifically combine the oxidizing of nitride disclosed by Eitan with the formation of the Hong nitride layer. Specifically, it is noted that in Hong the ONO stack is the dielectric between the control gate and the floating gate. In contrast in Eitan, the ONO structure is underneath the gate electrode. There appears to be no disclosure in Eitan of forming the gate structure overlying the ONO stack. See Eitan, col. 2, beginning line 34 through lines 42:

The method includes the steps of a) creating an oxide-nitride-oxide (ONO) layer on a substrate; ... e) forming rows of polysilicon or polysilicide perpendicular to and on top of the bit line oxides and ONO columns (emphasis added).

The motivation suggested by the Examiner is apparently merely that it is possible indeed to oxidize nitride in an ONO stack as taught by Eitan. There is no indication of why would one introduce this into the Hong inter-gate dielectric ONO layer. The Examiner does not indicate that any particular properties suggested by Eitan as a result of oxidizing the nitride would be useful in the Hong device or why such a step, for instance, would provide better performance or yield. Instead, apparently it is merely possible to do so according to the Examiner. It is clear under the standard of *In re Lee*, as referred to above, that this is insufficient motivation. Some actual motivation must be stated in the cited prior art. Hence the rejection of Claim 10 under 35 USC § 103 is traversed as relying on an insufficiently motivated combination of the two references, Eitan and Hong.

For similar reasons, if the Examiner were to consider rejecting amended Claim 1 under § 103 citing Eitan and Hong, it is submitted that such a combination is inadequately motivated and hence such a rejection is *prima facie* unsupported and improper.

Hence Claim 10 is allowable, as are dependent Claims 11-16.

Hence it is requested this case be passed to issue with earlier pending Claims 1-16 as amended allowed and new Claims 22-27 added, and already indicated as being allowable by the Examiner. If the Examiner contemplates other action, please contact the undersigned at (408) 453-9200.

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Respectfully submitted,



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**Appendix A - Version with markings to show changes made**

(In the appendix, added material is underlined, and deleted material is in brackets.)

1. (Amended) A method of forming a dielectric structure for a flash memory cell, the method comprising:

forming a first layer of silicon dioxide overlying a gate electrode of the flash memory cell;

forming a silicon nitride layer on the first layer of silicon dioxide;

[pretreating the silicon nitride layer including] oxidizing the silicon nitride layer; and

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer after the oxidizing.

2. (Amended) The method of claim 1, wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min.

3. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs at a pressure of approximately 1 atm. to 10 atm.

4. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

5. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% steam to 100% steam.

6. (Amended) The method of claim 1, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s.

7. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs at a pressure of approximately 1 atm. to 10 atm.

8. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

9. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 1% steam to 10% steam.

10. (Amended) A method of making a flash memory cell including [a substrate, a tunnel oxide and] a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer [nitride] on the first layer of silicon dioxide;

[pretreating the silicon nitride layer including] oxidizing the silicon nitride layer; and

depositing a second layer of silicon dioxide on the [pretreated] silicon nitride layer after the oxidizing.

11. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

12. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a batch furnace with a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% steam to 100% steam and a diluent, the diluent comprising one of argon and nitrogen.

13. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

14. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for

approximately 0.1 s to 6 s with a gas mixture of approximately 1% steam to 10% steam and a diluent, the diluent comprising one of argon and nitrogen.

15. The method of claim 10, wherein the first layer of silicon dioxide is approximately 40Å to 70Å thick, the silicon nitride layer is approximately 50Å to 150Å thick, and the second layer of silicon dioxide is approximately 30Å to 50Å thick.

16. The method of claim 10, further comprising forming a second polysilicon layer on the second layer of silicon dioxide.